IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

1. (Currently amended) A design method for an integrated circuit having a logic circuit, comprising:

a first step of converting a first netlist, which has connection data for a logic circuit in which a plurality of standard cells including at least a first flip flop are connected, into a second netlist by converting the first flip flops into second flip flops equipped with a scan function and adding scan chain interconnects that connect the second flip flops;

a second step of generating a third netlist by substituting the second flip flops in the second netlist for a plurality of standard cells that constitute the second flip flops, and generating scan-chain interconnect data;

a third step of performing layout of the standard cells and interconnects thereof which are contained in the third netlist, in accordance with the third netlist, optimizing an order of the scan chain interconnects on the basis of the scan chain interconnect data, and generating scan-chain interconnect order data; ~~and~~

a fourth step of generating a fifth netlist, from a fourth netlist that includes the second flip flops, and scan chain interconnects that depend on the scan-chain interconnect order data, by substituting the second flip flops for a plurality of standard cells, and of performing layout of the standard cells and interconnects thereof which are contained in the fifth netlist, in accordance with the fifth netlist; and

a step of generating logic circuit test patterns on the basis of the fourth netlist, wherein:

the standard cells are registered in a layout library as hard macros that contain layout information, and the layout of the standard cells is performed in the fourth step with reference to the layout library, and

the second flip flop having the scan function is not registered in the layout library as a hard macro that contains layout information.

2. (Cancelled)

3. (Currently amended) The design method for an integrated circuit as claimed in claim ~~2~~1, wherein the test patterns include an input test pattern that is inputted to the second flip flops in the logic circuit, and an expected-value test pattern, which is expected to be outputted by the second flip flops after a predetermined cycle operation.

4. (Currently amended) The design method for an integrated circuit as claimed in claim ~~2~~1, wherein the second flip flops and standard cells contained in the fourth netlist are registered in a logic library that contains logic information, and reference is made to the logic library in the test pattern generation step.

5. (Original) The design method for an integrated circuit as claimed in claim 1, wherein the fourth netlist is formed by converting the first flip flops contained in the first netlist into second flip flops and adding scan chain interconnects that depend on the scan-chain interconnect order data.

6. (Cancelled)

7. (Cancelled)

8. (Currently amended) A design method for an integrated circuit having a logic circuit, comprising:

a first step of converting a first netlist, which has connection data for a logic circuit in which a plurality of standard cells including at least a first flip flop are connected, into a second netlist by converting the first flip flops into second flip flops equipped with a scan function and adding scan chain interconnects that connect the second flip flops;

a second step of generating a third netlist by substituting the second flip flops in the second netlist for a plurality of standard cells that constitute the second flip flops and performing optimization by substituting the substitute standard cell and neighboring standard cell for a different standard cell of a smaller surface area; and

a third step of performing layout of the standard cells and interconnects thereof which are contained in the third netlist, in accordance with the third netlist, wherein:

the standard cells are registered in a layout library as hard macros that contain layout information, and the layout of the standard cells is performed in the third step with reference to the layout library, and

the second flip flop having the scan function is not registered in the layout library as hard macro that contains layout information.

9. (Original) The design method for an integrated circuit as claimed in claim 8, wherein the standard cells are registered in a layout library as hard macros that contain layout information, and the optimization involving substitution for different standard cell is performed in the second step with reference to surface area information of the layout library.

10. (Cancelled)

11. (Cancelled)